MicroLAN Design Guide

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What is the MicroLAN?

The MicroLAN is a low-cost network based on a PC or microcontroller communicating digitally over twisted-pair cable with 1-Wire ™ components. The network is defined with an open drain (wired-AND) master/slave multidrop architecture that uses a resistor pull-up to a nominal 5V supply at the master. A MicroLAN-based system consists of three main elements: a bus master with controlling software, the wiring and associated connectors and 1-Wire devices. Any standard microcontroller such as an 8051 with at least a 1.8MHz clock, as well as a PC using a 115.2 kbps-capable UART, can serve as master for the MicroLAN. The UART supplies 1-Wire timing by sending a byte for each 1-Wire bit, creating within the byte short and long time slots to encode the binary 1's and 0's. At this 14.4 kbps data rate (115.2 divided by 8 = 14.4 kbps) the PC can address a node on the bus and start receiving data in less than 7 milliseconds. Since timing is controlled by the UART, microprocessor clock speed does not affect the search time. Software such as TMEX™ to control and monitor bus activity is available and is included with the DS0621-SDK Software Developer's Kit .

MicroLAN protocol uses conventional CMOS/TTL logic levels, where 0.8V or less indicates a logic zero and 2.2V or greater represents a logic one. Operation is specified over a supply voltage range of 2.8 to 6 volts. Both the master and slaves are configured as transceivers allowing data to flow in either direction, but only in one direction at a time. Technically speaking, data transfers are half-duplex and bit-sequential over a single pair of wires, data and return, from which the slaves "steal" power by use of an internal diode and capacitor. Data is read and written least significant bit first. An economical DS9097 COM Port Adapter is available to interface RS-232 to the MicroLAN. Newer more versatile adapters based on the DS2480 Serial 1-Wire Line Driver chip provide more capability such as active pull-up and slew-rate control. The DS2480 is designed to interface between RS-232 and the 1-Wire bus, generating the proper signals and programmable waveforms that provide maximum performance. Regardless of whether a DS9097- or a DS2480-based adapter is used, readily available, low-capacitance, unshielded, Category 5 twisted pair phone wire is recommended for the bus.

As previously mentioned, data on the MicroLAN is transferred with respect to time slots. For example, to write a logic one to a 1-Wire device, the master pulls the bus low and holds it for 15 microseconds or less. To write a logic zero, the master pulls the bus low and holds it for at least 60 microseconds to provide timing margin for worst case conditions. A system clock is not required, as each 1-Wire part is self clocked by its own internal oscillator that is synchronized to the falling edge of the master. Power for operation is derived from the bus data line by including a half-wave rectifier onboard each slave. In *Figure 1*, whenever the data line is pulled high by the bus pull-up resistor the diode in the half-wave rectifier turns on and charges the internal 800pF capacitor. When it drops below the voltage on the capacitor, the diode is reverse-biased, isolating the charge. This isolated charge stored on the capacitor provides the energy source to power the slave during the intervals the bus is pulled low. The amount of charge lost during these periods is proportional to the time the bus is low. It is replenished when the data line again turns on the half-wave rectifier diode. This concept of "stealing" power from the data line by a half-wave rectifier is referred to as "parasite power."

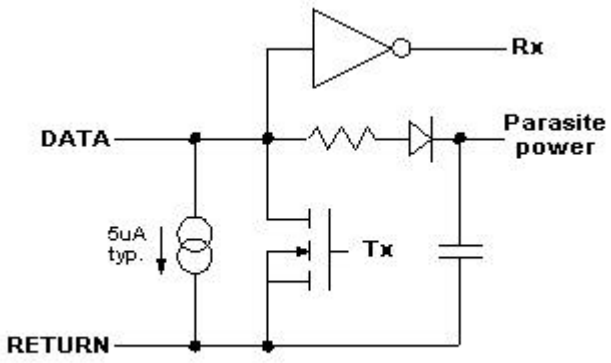

Figure 1: 1-Wire parasite power circuit.

In operation, the master resets the network by holding the bus low for at least 480 microseconds, releasing it, and then looking for a responding presence pulse from a slave connected to the line. If a presence pulse is detected, it then accesses the slave by calling its address. The master issues any device specific commands required, and performs any needed data transfers between it and the slave. It controls the information transfer by generating time slots and examining the response from the slave. For a more detailed description of the communication sequence, refer to "So that's how it works!" in the Appendix. Complete technical and timing details are available in the *Book of DS19xx iButton Standards*. (Contact Literature.Request@dalsemi.com for a copy.)
The address of each device is stored in a lasered ROM section with its own guaranteed unique, 48-bit serial number that acts as its node address. With 2^{48} serial numbers available, there will never be a problem with conflicting or duplicate node addresses on the LAN. This 48-bit serial number is just part of a 64-bit code programmed into each 1-Wire device at the factory. An 8-bit family code is stored in the first byte that identifies device type. The next 6 bytes store the unique individual serial number while the last byte contains a cyclic redundancy check sum (CRC) with a value based on the data contained in the first seven bytes. This allows the master to determine if an address was read without error.

Floppy in a Button

1-Wire devices can be formatted with a file directory just like a floppy disk. This allows files to be randomly accessed and changed without disturbing other records. Information is read or written when a device fixed somewhere along the bus is addressed by the master, or an identification badge or Decoder Ring is touched to a port somewhere along the MicroLAN. A typical access port consists of outer ring and insulated spring-loaded center conductors mounted in an appropriate housing. The outer ring touches the case of the iButton or Decoder Ring and connects it to the return line of the bus. The spring-loaded center contact touches the lid and connects it to the bus data line.
The inclusion of memory in 1-Wire chips allows standard information such as employee name, ID number etc., to be stored within the device, with up to 64K available. For example, it would only take about one-fourth of the available memory to store the equivalent of a business card and digitized black and white ID photograph. This still leaves generous space for additional important data such as medical records, credit information or security level to be included. With such information literally "at hand" in the case of the Decoder Ring, reliable identification and access is readily available and machine readable.

Packaged and ready to go

Because the MicroLAN only requires one wire plus return, iButtons can be packaged in a coin style battery case 16mm in diameter and 5.8mm thick. This is about the size of a stack of three dimes. The two-piece stainless steel package acts as both protective housing and electrical connection point. The case serves as return contact (ground) and the lid as data contact. The package size allows inclusion of a Lithium cell to provide 10 years of standby power to maintain data in volatile RAM memory when not connected to the LAN. A variety of memory configurations are available, including iButtons containing up to 64K of memory. 1-Wire devices that do not require a memory backup battery are also available in more traditional solder-mount packages.

SECTION 2: Working the LAN

Control the slew rate of the driver

In a typical system using a PC running Dallas' 1-Wire Operating System Software (TMEX) and using a COM port adapter, communication occurs in time slots of 8.68 microseconds under control of the UART. A communication cycle begins when the transistor in the master actively pulls the line to a logic zero. This one to zero transition is the synchronizing edge for all MicroLAN communications. A 1-Wire slave holds the zero if appropriate, and the resistor returns the line to the supply voltage after both the master and slave release the line. In ROM search, which is required to identify the devices on the bus, the most critical part of 1-Wire communication is the read data time slot, especially if a one is being transmitted. In the general case, there may be many arbitrarily placed devices on the bus. Each sees the falling edge of the time slot issued by the master at a slightly different time. Because communication requires that a signal travel the length of the cable and return, the electrical length of the bus must be less than one-half the time interval allowed for a single data bit slot. That is, round trip propagation time for a signal must be less than 4.34 microseconds (8.68 microseconds divided by 2). Devices beyond this range will not be seen by the master.

At the master, there is an active pull-down transistor that is either turned fully on or completely off under control of the PC or microprocessor. The falling edge generated by turning it on signals the start of a time slot on the MicroLAN. When the switch is turned off, the line is pulled toward the supply voltage by the bus pull-up resistor. Due to the rapid response and low impedance of the active pull-down transistor used to generate a logic zero, the signal fall time will be in the sub-microsecond range. If switching occurs in less time than the transition takes to traverse the electrical length of the cable and return, the MicroLAN is operating in a transmission line environment and reflections from the line end can cause bit errors.

Normally, the solution would be to terminate the ends of the cable in its characteristic impedance with fixed resistors. These resistors would then absorb the energy that otherwise would be reflected by the impedance mismatch and cause problems. However, the recommended cabling has a 100 Ohm typical impedance which would result in the inability to generate a logic one with an acceptable pull-up resistor. It is interesting to note that since the port transistor inside 1-Wire devices has a 100 Ohm on-resistance, the bus is properly terminated anytime one at the cable end is turned on. It may be possible on some MicroLANs to AC terminate the bus using a series resistor and capacitor connected to ground. After the capacitor charges, it blocks DC current so the series resistor presents no load to the bus. During transitions however, the capacitor appears as a short circuit and the resistor terminates the line. A general rule of thumb for selecting the capacitor, is 3 times the rise time divided by cable impedance. For a 4 microsecond rise time on 100 Ohm cable, this works out to be 0.1µF. This termination works best with low inductance cables.

Consequently, because it is not possible to permanently terminate the end of the MicroLAN cable in its characteristic impedance with a fixed resistor, the slew rate of the bus master pull-down transistor must be controlled. A 1.1 volt per microsecond slew rate is recommended for bus lengths of 100 meters or more. This provides a one to zero transition that takes about 4 microseconds to ramp to the 0.8V logic low threshold. Because port transistors in 1-Wire devices only hold the line down after the bus master pulls it low, they do not normally exhibit slew rate problems. The exception is when they exert a presence pulse in response to a Reset command.

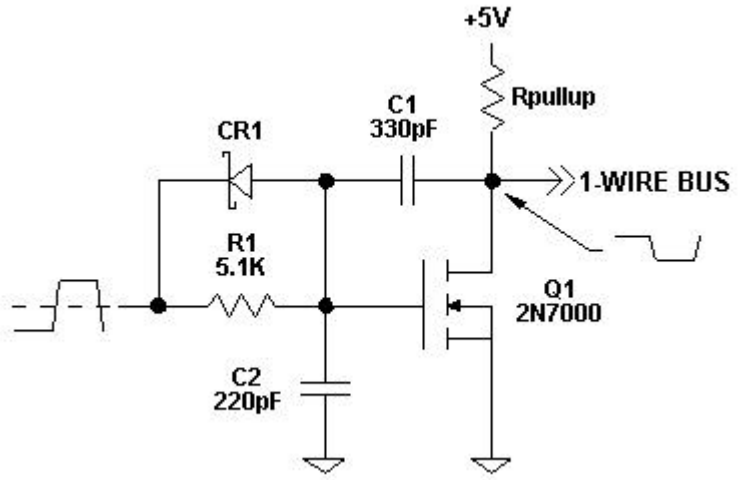

Figure 2: A controlled slew rate pull down for the MicroLAN bus master. Transistor type is not critical.

Figure 2 shows a suggested slew rate control circuit. The 2N7000 shown, is a commonly available general purpose n-channel FET, but transistor characteristics are not critical and almost any general purpose n-type transistor may be substituted. A bipolar type such as the 2N2222 may also be used with minor component value changes to provide the recommended slew rate. Refer to the Appendix for additional information and a 1-Wire waveform template.

Pulling up the line

Once both master and slave turn off, the bus pull-up resistor pulls the data line high. As the capacitive load on the MicroLAN increases by adding 1-Wire devices, the time to raise the data line to the supply voltage also increases. This also occurs when the network is lengthened due to the 50pF of capacitance added per meter of twisted-pair cable. This can be seen in *Figure 3* as the number of slaves is increased from 1 to 300. If the product of the total capacitive load (including cable, device, stray capacitance, etc.), and the pull-up resistor value results in a time constant (RC) that exceeds the bit time slot defined by 1-Wire protocol, communication stops. Because grounding unused wires or shields in a cable adds capacitance which can significantly increase the RC time constant, they should be left disconnected.

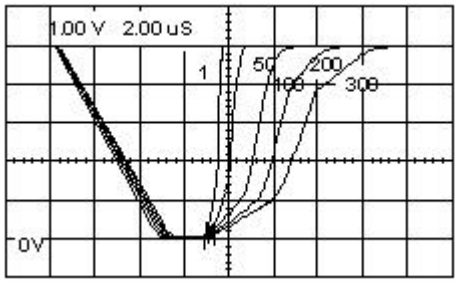

Figure 3: Loading effect of increasing the number of 1-Wire devices using active pull-up and 2m cable.

As can be seen in *Figure 5*, the input capacitance of 1-Wire devices contribute to the capacitive load on the network. However, the 800pF parasitic power supply capacitance only exists at voltage levels above 2.8V minimum. Ignoring the capacitance of the parasitic power capacitor, the bus pull-up resistor value, together with the cable capacitance and 1-Wire device input capacitance represent the network time constant ***t***. This omission is reasonable since parasite capacitance does not become a factor until the bus has already passed the 2.2V logic one threshold. The network time constant determines the rate at which the data line returns to a logic one voltage. With the requirement that at *t equals 13.02 microseconds* (the data sample time) the 1-Wire voltage needs to have reached the 2.2V threshold of a logic one, the value of ***t*** can be calculated as follows:

$$t = 13.02\ \mu s / \ln (Vs/(Vs-2.2V))$$

Where Vs is the pull-up supply voltage. Using the recommended 1.5K minimum pull-up resistor value and 5V supply voltage, ***t*** is calculated as 22.4 microseconds. Assuming the MicroLAN is loaded with the maximum fanout as calculated in a later section, the cable capacitance alone must not exceed 12nF to yield a network time constant no more than calculated. Using 50 pF/m as typical cable capacitance implies that the theoretical maximum cable length is 240 meters. This can be extended roughly 1 meter for every two 1-Wire devices less than the fanout maximum. The effect of cable capacitance can be seen in *Figure 4*, where 100 1-Wire devices were addressed at the end of a 2 or 100 meter cable. The 100 meter cable added 5000pF of capacitance.

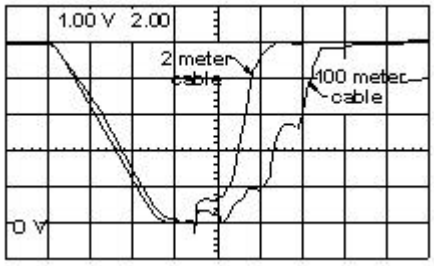

Figure 4: Effect of cable capacitance on signal driving 100 1-Wire devices. The 100m cable adds 5nF.

The risetime can be improved by reducing the value of the pull-up resistor, using lower capacitance cable, shortening the cable, or reducing the number of devices on the bus. The pull-up resistor, however, should not be reduced below 1.5K Ohm. Reducing the value of the pull up resistor increases the logic zero voltage on the network,

reducing system noise immunity. If the value of the pull-up resistor is already minimum, an active pull-up may be substituted. This also allows use of longer cables by decreasing the network time constant. Of course, the same rules apply to an active pull-up as to a pull down, and slew rate must be controlled when operating in a transmission line environment. The effect of residual current flowing in the bus when the active pull-up turns off can be seen in *Figure 7*. This was of little concern with a passive pull-up as an RC time constant has an inherently slow slew rate.

An active pull-up

One convenient source of an active pull-up is the MAX6314. This part was designed by MAXIM as a bidirectional open-drain µP reset for the 68HC11. However, it contains circuitry to automatically enable a p-FET 20mA pull-up for 2 microseconds when the data line exceeds a trip voltage of about 0.6V on the rising edge. Unfortunately, it does generate a logic zero output whenever the supply voltage drops below its reset threshold (its intended use). For use on the MicroLAN this can be detrimental as heavily loaded data lines can cause a reset, disabling communication, so selection of a part with a low reset threshold is suggested. One possibility is the MAX6314US31D3-T. This part has a 3-volt trip level that allows the supply to drop 2 volts before it generates a reset. The MAX6314 comes in a four-pin SOT143 package that requires little PCB area.
Although the MAX6314 contains an internal 4.7K pull-up resistor, it is recommended that an external 2.2K resistor be used in parallel. This provides the equivalent of the recommended minimum 1.5K pull-up resistor, which results in the bus crossing the trip voltage in minimum time. The bus waveform then exhibits three distinct segments. When both the master and the 1-Wire devices release the data line, it starts rising at a rate determined by the value of the pull-up and the total capacitive load (RC time constant). When it passes its trip threshold of approximately 0.6V, the 20mA p-FET is turned on and accelerates the bus toward the supply voltage. If the bus is heavily loaded, the 2 microsecond one-shot may timeout with the bus well below the supply voltage. If this occurs, the 1.5K equivalent pull-up resistor continues to raise the bus voltage at the rate seen when the bus was first released. All three of these segments can be seen in *Figure 3*. This data however, was taken with a discrete proprietary design and not with the MAX6314. For additional design information on active pull-ups refer to the Appendix.

Max Fanout

The maximum voltage to which the bus pull-up resistor can raise the data line is determined by the product of the pull-up resistor value and the idle current of all devices on the line. The more devices, the greater the voltage drop across the pull-up resistor. The fanout limit of a particular MicroLAN is reached as the voltage drop across the pull-up resistor reduces the MicroLAN supply voltage to 2.8V. This is the minimum voltage that will recharge the parasitic power supply of the 1-Wire devices. From this, the maximum theoretical fanout may be calculated. It is equal to the supply voltage (Vs) minus 2.8V (the minimum operating voltage) divided by the pull-up resistor value. The resultant is divided by 15µA, the worst case device supply current. For a 5V supply and 1.5K minimum pull-up resistor value we have the following:

$$Fanout_{MAX} = (5\text{-}2.8)/1.5K = 14.67mA/15\mu A = 98 \text{ devices}$$

This represents the theoretical maximum number of 1-Wire devices that can successfully communicate with the master using a 1.5K pull-up resistor and 5V supply over worst case conditions of current and temperature. The assumptions being that all devices are drawing the maximum supply current and operating in a -40°C to 85°C environment. In the real world, all devices will only be drawing the 15µA maximum supply current during System Reset and Presence Detect. At that time all device oscillators turn on for 5T times. Since 1T time typically lasts 30 microseconds, 5T times represents 150 microseconds, with a worse possible case of 255 microseconds. Circuit design ensures that all 1-Wire devices will be able to operate from their internal parasite power source for the duration of this interval once fully charged. Thereafter, they will be drawing 5µA maximum which permits tripling the previously calculated fanout of 98. In addition, most systems will be operating over a much narrower temperature range which allows still larger fanouts. For example, in a typical lab environment, over 500 1-Wire devices in continuous communication had only a 1.2V drop across the pull-up resistor. This implies that typical idle current per device is less than 2µA when environmental and supply ranges are limited.

SECTION 3: It's all in the cable

Take care in selecting a cable

As previously mentioned, the MicroLAN consists of three segments: a bus master, the wiring and connectors and the 1-Wire devices as shown in the electrical equivalent circuit of *Figure 5*. The wiring between the master and the 1-Wire devices is modeled by the inductance and resistance of the data and return lines and the lumped capacitance of the cable. Cable capacitance is simply the product of cable length times unit capacitance. This is typically 50pF/m for the recommended Category 5 twisted-pair cable. Similarly, line resistance represents cable length multiplied by the specified resistance per meter of a single wire. A 1-Wire device is modeled by its input capacitance (Cin), a constant discharge current (Idisc), the parasitic power supply circuitry (Di, Ri, Cload) and its operating current (Iop) of 10 µA during communication. The 5µA idle current per 1-Wire device is required to keep its interface synchronized with the communication protocol. When the 1-Wire port transistor is on, its impedance is nominally less than 100 Ohm, which provides a 0.4V logic zero with a 4mA current sink. If multiple 1-Wire devices are residing on the bus, Cin, Idisc, Iop and Cload should be multiplied by the number of devices to determine the total. Ri needs to be divided by the number of devices. The port transistor inside the 1-Wire device allows it to place a logic zero on the network. Except for the presence detect cycle, Search, Skip and Read ROM commands, only one of them will be conducting when addressed by the bus master.

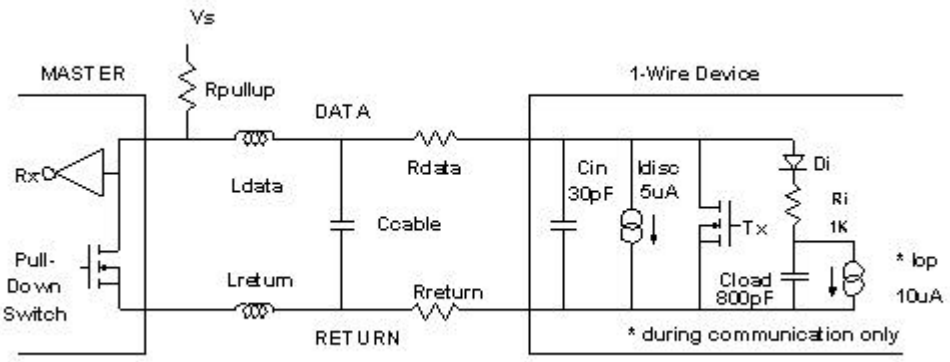

Figure 5: Electrical equivalent circuit of the MicroLAN.

While parasitic resistance reduces the zero logic level noise margin of the digital signals, cable capacitance together with the parasitic power supply of 1-Wire devices adversely affect the size of the network. At power up, this capacitive loading requires several milliseconds to charge before communication can start on the MicroLAN, especially if a passive (resistive) pull-up is used. Also on long lines with many 1-Wire devices grouped at the end, the parasitic power requirements create a dip or slope change in the rising edge of the waveform at about 2.8V as the energy reservoirs of the devices are filled. Once filled, the recovery time after each time slot will be sufficient to maintain the charge. *Figure 6* shows the effect charging the parasite power capacitance has on different numbers of 1-Wire devices at the end of 100 meters of Category 5 cable. Notice that the slope of the rising edge decreases as it crosses the 2.8V threshold finally reversing direction to form a dip when loaded with 100 or more devices. These "dips" become more pronounced the longer the bus remains low.

Clearly the physical properties of the cable connecting the master and 1-Wire devices strongly affects and limits the MicroLAN network. Comparison of the waveforms of *Figure 3* taken with two meters of Category 5 cable to those of *Figure 6* taken with 100 meters makes this plain. For short runs up to 30 meters, cable selection for use on the MicroLAN is less critical as the impedance characteristics are generally insufficient to have a marked adverse effect on the bus. Even flat modular phone cable works with limited numbers of 1-Wire devices. However, the longer the MicroLAN, the more pronounced cable effects become, and therefore the greater importance placed on cable selection.

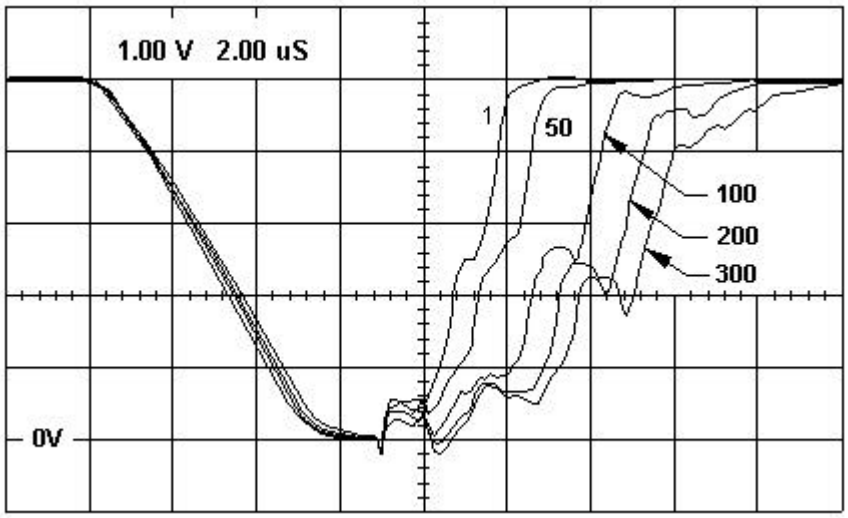

Figure 6: Parasite power loading of 0 to 1 transition. Notice that the dip becomes more pronounced with increasing number of devices at end of 100m cable.

Given sufficient length, any cable exhibits transmission line effects. Real cables display distinct properties of resistance, capacitance and inductance, which in turn are determined by cable geometry, the size and spacing of the conductors and their surrounding dielectric. These physical properties define the characteristic impedance, the signal bandwidth supported and the propagation velocity of the cable. Specifically, cable resistance reduces the zero logic level noise margin, although values to 100 Ohms for the total cable length are acceptable. Cable capacitance however, which can range from 30pF/m to 100pF/m, loads the MicroLAN driver, increasing not only the network time constant (***t***) computed earlier, but also the peak current flowing in the cable as the master transistor turns on and discharges the line.

If this transistor turns off before the charge stored in the line capacitance is completely discharged, the residual current left flowing in the line determines the amplitude of a transient voltage spike generated as a product of this current and the cable inductance. The resulting voltage spike seen at the driver can become large enough to interfere with communication. The effect of residual current flowing in the cable when the bus pull-down transistor and the active pull-up turns off can be seen in *Figure 7*. Notice that in each case, the spike generated is in the direction of the opposite rail.

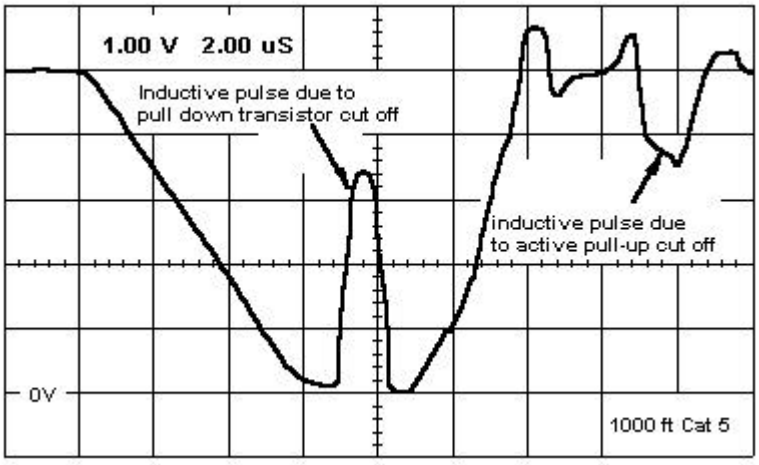

Figure 7: Inductive generated voltage spikes such as seen here, may occur on long lines due to residual current flow when pull down or pull-up circuits turn off.

At the far end of the cable, when the pull down transistor turns off its inductively generated voltage spike swings negative, reverse biasing the substrate of the 1-Wire device closest to the cable end which clamps the voltage excursion at a diode drop. This device then will not respond to the master.
The problem is the differential inductance, which is that measured across the cable input when the two wires of the line are shorted together at the far end. Differential inductance is substantially lower than the inductance of a single wire because the current flows in opposite directions in the pair and in the ideal case would cancel completely. Because differential inductance decreases as the distance between conductors is reduced, use of adjacent and preferably, twisted pair is recommended. Twisted pairs help reduce unwanted coupling from nearby interference sources because the currents induced in the wires flow in opposite directions in the two conductors and tend to cancel.
Another consideration is that the recommended category 5 unshielded twisted pair phone cable is available with two or more pairs. While the capacitance between wires in a pair is approximately 50 pF/m; that between wires of different pairs is closer to 30 pF/m. Because grounding the unused wires will add this 30 pF/m to the 1-Wire capacitive load, shields and unused wires need to be left unconnected at both ends of the cable. Grounding them can increase the capacitive load to the point that the bus pull-up cannot raise the line above the logic switching threshold within the bit time slot and communication stops. Refer back to Section 2 and the discussion of network time constant in "Pulling up the line" for more information. It is also not recommended to simultaneously run two MicroLANs in the same cable bundle, because the capacitive load varies dynamically dependent upon data pattern, which can lead to erratic operation.

Keep the bus running

As line inductance increases, the product of L di/dt can generate voltage excursions that cause bit errors and reverse bias the substrate of at least the first 1-Wire device at the far end of the cable. These voltages spikes are generated by the current still flowing in the data and return lines of the cable when the transistor in the master is turned off before the charge stored in the line capacitance is fully discharged. The obvious and recommended solution is to maintain the pull-down transistor in the on state until the current in the line discharges. If it is not possible to stretch the timing, a Schottky diode placed across the bus at the far end is suggested to clamp the inductive generated voltage overshoot. Connect the diode across the cable with the cathode on the data line, and the anode on the return. Only one diode is required for each length of MicroLAN branch.

Sample later

When a PC with 115.2 kbps UART is used as the bus master, the MicroLAN time bit slot is the reciprocal or 8.68 microseconds. Because it is preferable to sample in the middle of a time slot away from logic transitions, the data line is sampled 13.02 microseconds (1.5 times the bit time) after the master pulls the line low. This means the bus pull-up must raise the line above the 2.2V logic one threshold within 4.34 microseconds (13.02 minus 8.68 equals 4.34). Since 1-Wire devices are guaranteed to provide a minimum 15 microsecond data bit, 13.02 microseconds is normally a good time to sample. However, with a heavily-loaded or long line, it may not be possible for the bus pull-up to raise the line before it is sampled by the master. Changing the sample time from 1.5T to 2.5T or 21.7 microseconds (8.68 times 2.5 equals 21.7) gives the bus pull-up more time to raise the line above the logic threshold. This timing change is acceptable if the environment is limited to a 0° to 50°C range with a 5V to 6V supply voltage. Dallas Semiconductor is in the process of tightening up 1-Wire specifications and making this timing change the standard. This will allow return to wider temperature ranges when using the new parts. Upgraded software will also be available that will include the sample time change.

SECTION 4: Rewiring the LAN

The DS2409 MicroLAN Coupler

If the network is heavily loaded, and/or very long, it may be preferable or necessary to separate the bus into sections. This has the added benefit of providing information about the physical position of a 1-Wire device on the bus. By using one section as the main "trunk," and adding or removing segment "branches" to it with a DS2409 as needed, a true MicroLAN is created. It is also possible of course to add or remove additional segments to the branches using a MicroLAN Coupler as the node control. This approach reduces the capacitive and idle current loads the bus master sees to that of the trunk and those segments connected to it by activated DS2409s. However, the limitations to the total capacitive load, idle current and line length covered in earlier portions of this document still apply. That is, for the trunk and activated sections of the LAN, the capacitive load must be low enough to allow the bus pull-up to raise the line above the logic one threshold within the time slot. The combined idle current of the 1-Wire devices must not reduce the supply voltage below 2.8V. And the electrical length of activated cable must allow a transition from the master to reach the cable end and return within the time slot.

The DS2409 MicroLAN Coupler is a key component for creating complex MicroLANs. It contains the MAIN and AUX transmission gate outputs, plus an open drain CONTROL output transistor, all of which can be remotely controlled by the bus master over the 1-Wire network. Both the MAIN and AUX outputs support a "smart-on" command which generates a reset/presence sequence on the selected output before connecting to the 1-Wire bus. This allows a subsequent ROM function command to apply only to the devices on the just activated segment. The DS2409 requires a 5V supply without which it shorts the 1-Wire bus and no communication is possible. Since the DS2409 contains no user-available memory, the AUX output can be used to label the node by connecting a 1-Wire memory chip to store the required data. A simple MicroLAN consisting of a single BRANCH and one LIMB with EEPROM labels and connected as just described is shown in *Figure 8*. The DS2409 is available in a 6-pin TSOC surface-mount package. Please refer to the datasheet for further information.

The DS2407 dual addressable switch

The DS2407 is a low-side addressable switch intended for remote control, perhaps in combination with an opto-coupler or relay, or to provide visual indication of an operation or end-of-limb by means of an LED (Light Emitting Diode). The DS2407 is ***not*** recommended as a means for providing branches on the MicroLAN, because branching requires use of a high side switch. This is because current flowing through the on-resistance of the port transistor develops a voltage that raises the ground pin of all devices connected to it above the ground reference. Since the 1-Wire devices will be hard wired to the data line, whenever the bus master outputs a logic zero the potential on the data pin becomes negative with respect to the voltage on its ground pin. This polarity acts to forward bias various p-n junctions in the 1-Wire devices resulting in device dependent disruptions. For example, when this voltage reaches approximately -0.3V, it can continuously activate the POR (power-on-reset) of any attached DS2407, effectively removing it from the bus.

The DS2407 addressable switch was designed to perform closed-loop control of its two open drain output transistors, PIO-A and PIO-B, over twisted pair cable up to 300 meters from a PC. Each output can also sense and report to the PC the logic level at its port. When turned on by the bus master, the PIO-A port is connected to the IC ground pin and can sink up to 50 mA, and hold off a maximum of 13V, while the PIO-B sinks 8 mA and holds off 6.5V. The on-resistance of the DS2407 PIO-A output transistor is about 10 Ohms, whereas the PIO-B output is about 50 Ohms. The off impedance of both addressable switches exceeds 10 Meg Ohms. The DS2407 is available in a 6-pin TSOC surface-mount package or as a single-channel (PIO-A) version in a TO-92 package. For more information on the DS2407 dual addressable switch which contains 1K of one time user programmable EPROM, please refer to the datasheet.

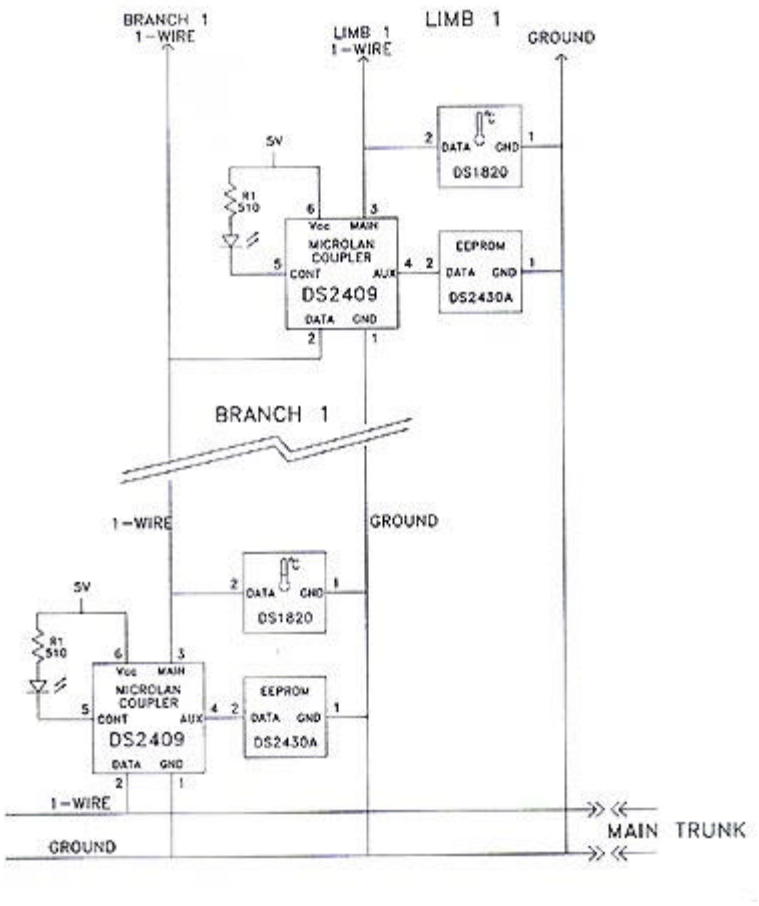

Figure 8: Separating the 1-Wire bus into branches using the DS2409 MicroLAN Coupler.

In this example, a DS2430 EEPROM is connected to the AUX output of each DS2409. This provides information specific to that particular node such as location, function, etc. An LED attached to the the CONTROL output provides visual indication of the specific node being addressed and can be caused to flash via software for extra visual impact. A single DS1820 Digital Thermometer is shown on the output of BRANCH 1 and LIMB 1 but multiple 1-Wire devices can be placed on each as required.

SECTION 5: Policing the LAN

Protection and Noise

All MicroLAN-compatible 1-Wire devices contain built-in ESD (electrostatic discharge) protection circuitry able to withstand ± 10kV minimum Human Body Model ESD events. However, when interfacing a computer to a MicroLAN it is good engineering practice to provide additional means to protect the system from ESD and EMI (electromagnetic interference) damage. Economical protection can be provided at the bus master by means of diodes shorting negative spikes or feeding positive ones higher than 5V to the power supply where they are absorbed by capacitors and other protection devices. When selecting protection diodes or surge suppressers, choose devices with minimum junction capacitance and fast switching times. Two good examples are the ERA82 Schottky diode from FUJI or the more common 1N5817.
If 1-Wire EPROM parts will not be programmed using the RS-232 to MicroLAN interface adapter, excellent protection can be provided with a single DS9502 ESD protection diode. These behave like a 7.5V zener diode during normal operation. However, if the voltage across them exceeds their 9V trigger voltage they fold back to 5.5V. If exposed to an ESD hit beyond their ratings, the DS9502 will eventually fail shorted, preventing damage to the protected circuitry. The DS9502 is available in a 6-lead TSOC package, or as solder-mount "bumped" die.

Introducing the DS2480

In order to reduce the engineering load of setting up a MicroLAN, Dallas Semiconductor has developed the DS2480 Serial 1-Wire Driver. This IC connects directly to UARTs and 5V RS-232 systems. Adapters are available using the DS2480 that connect directly to a standard COM port and provide 1-Wire outputs. The IC contains programmable pull-down slew-rate control and an active pull-up. Other features include support for data rates of 9.6 (default), 19.2, 57.6 and 115.2 Kbps and programmable 1-Wire timing.
The DS2480 is available as the DS9097U-S09, which is a DB9 to RJ11 COM port adapter, the DS1411 with a DB9 to DS9098 iButton socket and the DS1416D with DB9 to dual blue dot receptors. These are true ground adapters, Crypto-capable with FCC Class B approval.

It's the results that count

By applying information presented in this tech brief such as using Category 5 twisted pair, controlling slew rates and substituting an active pull-up, reliable communication over 300m of cable with more than 500 assorted 1-Wire devices was demonstrated. Without slew rate control and active pull-up, the limit is about 100 meters with 150 1-Wire devices.

Recommendation summary for operating long or heavily loaded MicroLANs
Select cable • Good: twisted-pair phone • Better: Category 5 twisted pair
Use a diode clamp • Use a Schottky diode across the cable's end. Connect the diode reverse-biased with the cathode on the data line and anode on the return.
Use multilevel branching • Use DS2409 MicroLAN Couplers to separate the MicroLAN into branches.
Use a DS2480-based COM port adapter • DS9097U-S09 DB9 to RJ11 adapter, *or* • DS1416D-DAA DB9 to dual Blue Dot Receptor, *or* • DS1411 DB9 to DS9098 socket adapter
If a DS2480-type adapter is not used
Control slew rate • Limit the slew rate of the pull down to about 1.1 volts per microsecond.
Use an active pull-up • Replace the pull-up resistor with an active pull-up, limiting slew rate to about 1.1 volts per microsecond.
Keep the bus running • Keep the bus master transistor on until residual line current dissipates.
Use later sampling • Use 21.7 microsecond timing (2.5T) instead of the normal 13.02 microsecond (1.5T) timing.

APPENDIX: Hardware for the MicroLAN

PC to MicroLAN adapters

Any PC with a UART capable of 115.2 kbps can serve as bus master for reading and writing 1-Wire devices on the MicroLAN. However, a serial COM port to MicroLAN adapter is needed to interface the computer RS-232 levels to the 5V 1-Wire bus. A schematic for the DS9097 COM port adapter developed by Dallas Semiconductor as an economic and easy to use interface, is shown in *Figure 9*. The adapter is powered entirely from the computer COM port. Note that the circuitry makes maximum use of the UART controlled output using only clamping and level shifting diodes. Although this provides a simple and reliable circuit that directly couples to the serial port, it lacks a ground reference. While not of concern in operating the MicroLAN, it can present complications during trouble shooting, as the oscilloscope ground cannot be connected to the 1-Wire return.

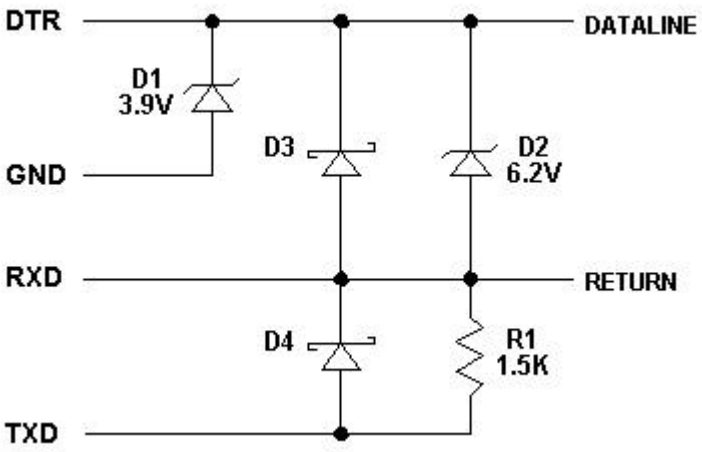

Figure 9: The DS9097 COM port adapter. Note that "return" is not ground. R1 is the bus pull-up.

In *Figure 9*, current limiting and slew rate control are provided by the UART as RS-232 requirements, while zener D1 clamps the data line at 3.9V. Zener diode D2 limits the maximum voltage range on the 1-Wire bus to 6.2V. It also restricts the most negative voltage swing on RXD to -2.3V. When TXD is positive, Schottky diode D3 limits the voltage difference between the 1-Wire data and return lines to 0.2V, and D4 connects TXD to RXD. This bypasses R1 the passive bus pull-up, and provides a low impedance path to initiate a time slot. The 1.5K minimum value pull-up resistor generates a 0.3V logic zero across the 100 Ohm on-resistance of a 1-Wire device. Since the maximum voltage still recognized as a logic zero is 0.8V, this leaves 0.5V of noise margin.
The DS9097 comes with a DB9 for attachment to a PC serial port and an RJ-11 for connecting to the MicroLAN. The same circuit is available in a DB9 to DS9098 socket as the DS1413. A DS9097E version is also available for programming EPROM based 1-Wire products such as the DS198x series. It provides a power jack to accept an external 12V auxiliary supply as required.

A true ground COM port adapter

If the return line of the MicroLAN must be grounded at some point, a true ground COM port adapter interface is required. The schematic for a true ground adapter is given in *Figure 10*. Its positive supply is derived from DTR and RTS by Schottky diodes CR1 and CR2, and filter capacitor C1. A well-regulated 5 volts is provided by the low dropout LP2980 voltage regulator as long as the COM port provides at least 5.1V. If the positive level of DTR and RTS drops below this the regulator drops out of regulation. CR3 and C3 provide the negative supply required by the DS275 RS-232 Transceiver Chip from TXD during read data and idle time slots. The DS275 connects directly to the MicroLAN and converts it's CMOS/TTL levels to the RS-232 levels required by the UART. If surface mount components are used, the circuitry will fit comfortably on a 0.6" by 0.9" printed circuit board. This can be mounted inside a DB9 female to RJ-11 PC adapter.

A slew rate controlled pull down

Because it is not possible to terminate the ends of the MicroLAN cable in its characteristic impedance, the slew rate of the bus transistor must be controlled to prevent adverse transmission line effects. For more information on this subject, refer back to Section 2 and "Control the slew rate of the driver." In *Figure 10*, transistor Q1 and the components associated with its gate, limit the slew rate to about 1.1 volts per microsecond. This provides a one to

zero transition that takes about 4 microseconds to ramp from the 10% to 90% points. This has proven to be adequate for MicroLAN cable lengths exceeding 300 meters. The 2N7000 shown is a commonly available general purpose n-channel FET, but transistor characteristics are not critical and almost any general purpose n-type transistor may be substituted. A bipolar type such as the 2N2222 may also be used with minor component value changes to provide the recommended slew rate.
In the pull-down circuit of *Figure 10*, Miller integrator capacitor C5 across Q1 acts as the primary slew rate control element. On lightly loaded LANs using about 50 devices on 50 meters or less of cable, it may be possible to eliminate C5. Sufficient slew rate control is then provided by R1 and C4. In operation, when TXD switches from its minus 12V rail to the plus 12V rail, the signal is passed to the gate of Q1 by input resistor R1. This transition is slowed and delayed slightly by the RC time constant of R1 and C4. When the voltage level at the gate reaches the threshold voltage of Q1, the transistor begins to turn on. The effect of the transistor turning on with C5 across its terminals results in a nearly linear voltage ramp from the supply voltage to ground. This one to zero transition on the bus is the synchronizing edge for MicroLAN communications. Q1 remains in the on state for the duration of time that TXD is held at plus 12V by the UART. Afterward, the bus is returned to the supply voltage by the action of pull-up resistor R2. Zener diode D1 serves several functions in the circuit. It protects the gate of Q1 by limiting positive voltage excursions to 12V, and negative ones to minus 0.6V. Gate input resistor R1 limits the current through the zener. The capacitance of D1 also adds to that of C4, helping control the transistor transition.
While they are not shown for clarity, good engineering practice would place reverse-biased Schottky diodes across the output of the circuit. One diode should be from the supply voltage to the data line, the other from the data line to ground. Use of ultra-fast low-capacitance Schottky diodes such as the ERA82 from FUJI is suggested.

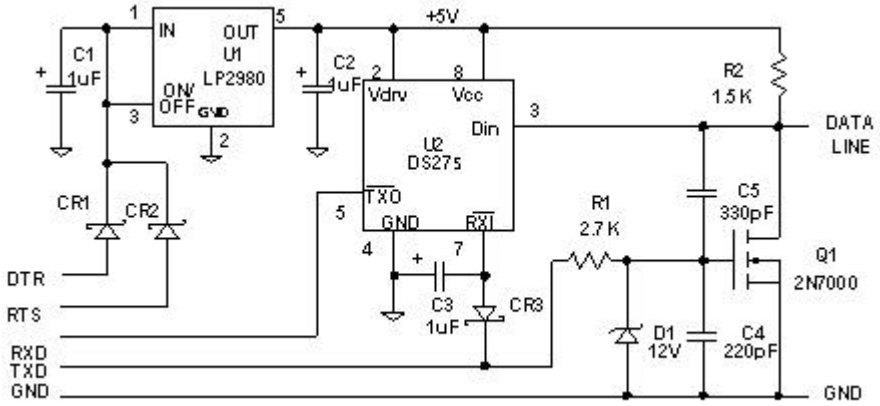

Figure 10: A PC serial COM port to MicroLAN true ground adapter. Q1 is the slew rate controlled pull-down and R2 is the passive bus pull-up resistor.

So that's how it works!

A cycle in the sequence of MicroLAN communication over the true ground COM port adapter would proceed as follows. Initially, TXD would be at minus 12V (an RS-232 "mark" or logic one), so the gate of Q1 would be clamped at minus 0.6V by the reverse bias on zener diode D1. Consequently Q1 is off, and the bus will have been raised to the 5V supply by pull-up resistor R2. When TXD switches between the minus 12V and plus 12V rails, Q1 will be turned on and ramp the bus voltage down at the rate set by the Miller integrator capacitor C5. This one to zero transition has two paths, one continues down the bus, the other returns to the UART through U2. The signal returned to the UART, will be used to determine when to reexamine its registers for a response from a 1-Wire device on the bus.
Meanwhile, the transition traveling down the bus is received sequentially by any attached 1-Wire devices as the edge propagates past them. If this signal from the UART is a Reset pulse, it lasts for at least 480 microseconds and then releases the bus. The bus pull-up raises the line to the supply, and approximately 30 microseconds later the UART reexamines its registers to see if a presence pulse is being sent by a 1-Wire device. In the interim, the internal oscillators and controllers within each 1-Wire device have determined that a Reset has been sent and at the appropriate time will pull the bus low. The exact time the bus is pulled low and its duration, is a function of individual device variation. The fastest will pull the bus low first, and the slowest release it last. When the final 1-Wire device releases, the pull-up resistor raises the bus toward the supply voltage at a rate determined by its value times the capacitive load it sees on the line (RC time constant). If the pull-up cannot raise the bus above the logic one threshold within the time slot, the master will always see a logic zero and conclude the line is shorted. Consequently, communication cannot occur. Assuming however that the timing is acceptable, the UART sees a proper Presence pulse indicating there are 1-Wire devices on the bus. It then proceeds to call serial numbers to identify them.

In order to write logic one or zero values onto the bus, the UART turns on Q1 for short (less than 15 microseconds), or long (greater than 60 microseconds) time slots respectively. To read, the UART begins by turning on Q1 for a short time slot exactly as if a logic one was being sent. If this time slot remains unchanged, the UART defines this as reading a logic one. If a 1-Wire device extends the time slot initiated by the master by continuing to hold the line low (even though the UART has released Q1 and R2 attempts to pull the data line high) the UART defines this as reading a logic zero.

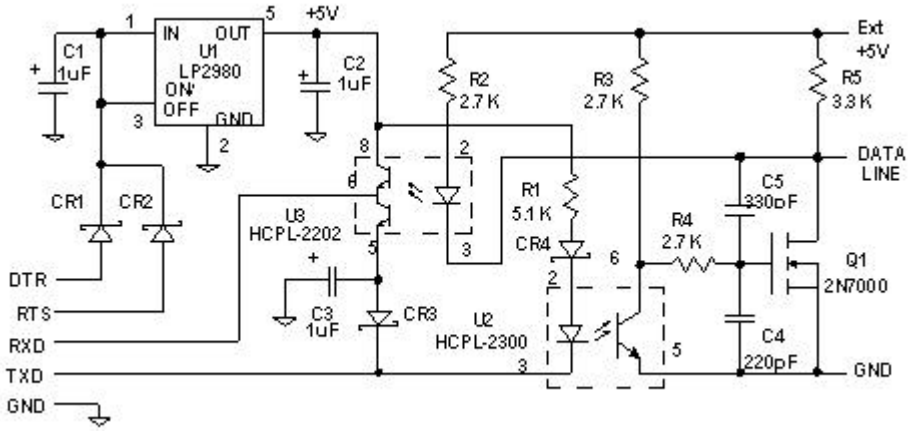

Figure 11: An optically isolated COM port to MicroLAN adapter.

An optocoupler-isolated adapter

In some applications, because of ground loops, or for safety reasons, it is necessary to provide galvanic isolation between the computer master and the MicroLAN. For such cases, the optically-coupled circuit in *Figure 11* is suggested. Optical isolation of the COM port requires special purpose optocouplers, such as the high speed, low input current HCPL-2300 used in the transmit section. An HPCL-2202 with 20V totem pole output is used in the 1-Wire to RS-232 channel.

The HCPL-2300 has an LED input that only uses 0.5mA, and an output transistor with 200 nanosecond maximum propagation time. In the circuit, the LED current is set with resistor R1, but a current source such as the J503 or CR056 from Siliconix will provide superior performance over the diversity of logic levels available with RS-232. If a constant current source is not used it may be necessary to recalculate the value of R1 to maintain 0.5mA with the plus and minus voltages in use on a particular RS-232 COM port. CR4 is required for reverse voltage protection of the LED, as it only has a 5V breakdown in the reverse direction.

In operation, the HCPL-2300 coupler U2, provides the necessary isolation and level shifting from the double rail plus and minus 12V RS-232 to the single rail MicroLAN. The coupler is connected in a non-inverting configuration, so when TXD is at minus 12V, the LED input is on. Consequently, the coupler output transistor is also on and the bus pull-down transistor Q1 is off. With Q1 off, bus pull-up resistor R5 holds the LAN at the supply voltage. U3, the receive optocoupler is also off, so its output is at minus 12V.

When TXD changes state, the HCPL-2300 input LED is reversed-biased, turning the coupler output transistor off. Its collector is then pulled high by resistor R3. This zero to one signal is slowed and delayed slightly by the RC time constant of R4 and C4. When the voltage level at the gate reaches the threshold voltage of Q1, the transistor begins to turn on. The effect of the transistor turning on with Miller capacitor C5 across its terminals results in a nearly linear voltage ramp from the supply voltage to ground. When Q1 pulls the data line to ground, it also turns on the LED in U3 the HCPL-2202 coupler, causing its totem-pole output stage to switch to plus 5V. This transition will be received by the UART and used to determine when to reexamine its registers for a response from any 1-Wire devices on the bus.

The data line remains at ground until TXD returns to its original state, and Q1 along with any 1-Wire slaves turn off. At that time, the bus pull-up resistors (R5 in parallel with R2) raise the data line toward the 5V supply at a rate determined by their equivalent value times the capacitive load seen on the line (RC time constant). This turns off the input LED of U3, and causes its output stage to switch to the minus RS-232 voltage level. Assuming the pull-up can raise the bus above 2.2V within the time slot, the UART will see a logic one, and communication proceeds. If the pull-up cannot raise the bus above the logic threshold within the time slot, the master will always see a logic zero and conclude the line is shorted. Consequently, communication stops.

An active pull-up

On a MicroLAN where the minimum acceptable pull-up resistor value cannot raise the data line above the logic one threshold within the time slot, an active pull-up must be used. Obviously, an active pull-up circuit should be on only during a defined range of the rising edge (zero to one transition). Conversely, it should not respond on the falling edge, nor be active during logic zero time intervals. It must trigger on the rising edge at about 0.9V plus or minus 0.1V to provide acceptable noise margin. Preferably, once triggered it will remain on until the line is raised above a specified threshold
(= or > 3V) rather than for a set time interval (one shot). This insures that the data line will be raised above the 2.8V level required to recharge the parasite power capacitors regardless of load. The maximum current supplied should be limited to about 15mA. Larger currents when flowing in cable inductance can cause problems. Refer to Section 3 "Its all in the cable" and see *Figure 7* for further information on the effects of cable inductance.
In Section 2 under "An active pull-up," use of the MAX6314 is suggested as an available circuit. This part was designed by MAXIM as a bidirectional reset intended for use with the 68HC11 microprocessor. As such, an important function of the chip is to monitor the supply voltage and assert a reset (logic zero) during power-up, power-down, or during supply droop. This obviously is an undesirable function on the MicroLAN. However, the part includes an active pull-up to solve the RC time constant problem faced on a high capacitance bus. Coincidentally, this consists of a p-FET in parallel with a 4.7K pull-up resistor (the maximum MicroLAN value). The FET is turned on for 2 microseconds when the waveform on the reset pin exceeds 0.9V maximum by a comparator triggered one-shot. Additional control circuitry ensures that the active pull-up is disabled at all other times.
Operation of the MAX6314 when connected to the MicroLAN bus proceeds as follows. When the bus (connected to the MAX6314 reset pin) is pulled below 0.5V by the master, a comparator sets an internal flip-flop enabling the active pull-up control circuitry. When the bus is released, the internal 4.7K pull-up resistor starts raising the bus toward Vs (the bus supply voltage) at a rate determined by it's RC time constant. This generates a ramp that starts at the logic zero level and ends at the trip voltage of a comparator. When the trip voltage of the active pull-up enable comparator is exceeded, it triggers a 2 microsecond one-shot that turns the 20mA p-FET on. This starts a second much steeper ramp that begins at the comparator trip voltage and ends at Vs. However, if the bus is heavily loaded, a third ramp may be created if the 2 microsecond one-shot times out, and the bus voltage has not reached Vs. This ramp starts where the one-shot times out, and ends at the maximum voltage to which the passive pull-up can raise the line with the idle current load of 1-Wire devices on the bus. This third ramp will have a slope similar to the first. The characteristic waveform produced by an active pull-up is illustrated in *Figure 12*.

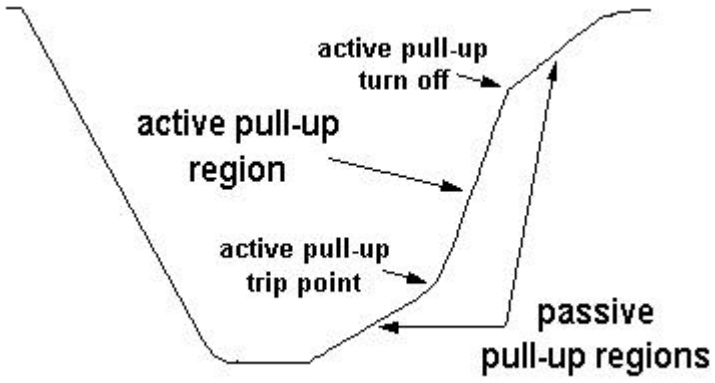

Figure 12: Characteristics of an active pull-up.

Although the MAX6314 contains an internal 4.7K pull-up resistor, it is suggested that an external 2.2K resistor be used in parallel. This reduces the value to the equivalent of the recommended 1.5K minimum pull-up resistor, and allows the bus to cross the enable trip voltage of the active pull-up in minimum time. The combination of the MAX6314 and 2.2K resistor can be substituted for R2 in *Figure 10* to provide a true ground COM port adapter with active pull-up.

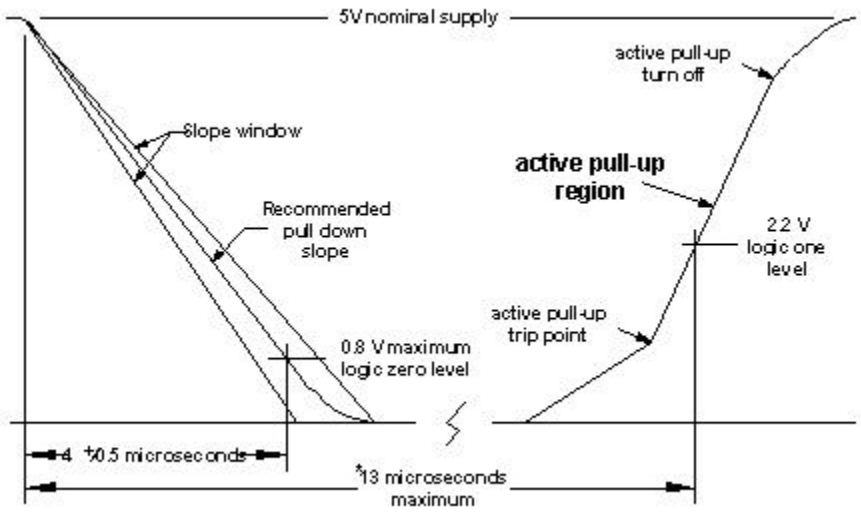

Figure 13: Waveform template for a MicroLAN bus exceeding 100 meters.

**21.7 microseconds for new 1-Wire devices*
This document defines the MicroLAN template for use with bus lengths extending 100 meters or longer. Notice that the zero to one transition is shown with the characteristic waveform for an active pull-up as the use of a passive pull-up resistor can be problematic with cables of this length. A 5V pull-up supply is recommended, but it can range from 3 to 6 volts.

The falling edge

The one to zero (falling) transition of the bus master pull-down transistor is the system timing edge. It should have a 1.1volt per microsecond (V/µS) slew rate. As shown in the template, this requires 4 microseconds to cross the 0.8V logic zero threshold level. This slew rate provides acceptable performance with MicroLAN bus lengths up to 300 meters. It performs well over that range with 1-Wire loading varying from one to 500 devices.
For communication over the MicroLAN to be successful, the bus must be raised to a voltage above the 2.2V logic one level before the master samples. With TMEX software through v2.1, sampling occurred 13.02 micro seconds after the master pulled the bus low. For version 3.0, sampling is at 21.7 microseconds. If the bus pull-up does not raise the voltage above the logic one threshold before sampling occurs, the master will always see a logic zero and conclude the bus is shorted. Consequently, communication can not occur.

The rising edge

As the number of 1-Wire devices on the bus grows, the time required to raise the line above the logic one threshold increases. This also occurs as the network is lengthened due to the 50pF of capacitance added per meter of twisted-pair cable. Because of these effects, for a MicroLAN of 100 meters or more, an active pull-up must be used. Obviously, an active pull-up circuit should be on only during a defined range of the rising edge (zero to one transition). Conversely, it should not respond on the falling edge, nor be active during logic zero time intervals. It must trigger on the rising edge at about 0.9V plus or minus 0.1V to provide acceptable noise margin. Preferably, once triggered it will remain on until the line is raised above a specified threshold (= or > 3V) rather than for a set time interval (one-shot). This insures that the data line will be raised above the 2.8V level required to recharge the parasite power capacitors regardless of load. The maximum current the circuit can supply should be limited to about 15mA. Larger currents flowing in cable inductance can cause problems.
Please consult the Dallas Semiconductor iButton website at **http://www.ibutton.com** for current product information, application notes and data sheets.